DAVID SIDLER

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EDUCATION

ETH, Zürich *April 2014 - Present*
Doctoral Studies, Computer Science
Advisor: Prof. Gustavo Alonso

ETH, Zürich *September 2011 - May 2013*
Master of Science,Computer Science
Focus: Information Systems

ETH, Zürich *September 2007 - September 2011*
Bachelor of Science, Computer Science

RESEARCH

My research consists of two main parts: **in-network data processing** and **database acceleration**.

In-network Data Processing
I am using reconfigurable hardware to explore what kind of data processing operations are potential candidates to be pushed closer to the network, in particular onto the network card. In my current project I use an FPGA to prototype an RDMA network card. The prototype features a RoCE (RDMA over Converged Ethernet) hardware implementation that can be extended with new RDMA verbs to explore new data flow and compute capabilities. In an earlier project I developed a complete TCP/IP stack for reconfigurable hardware.

Database Acceleration
In my research I explore how to use CPU-FPGA hybrid architectures to accelerate and extend relational databases. In our project, *doppioDB*, we accelerate regular expression matching by using runtime-parameterizable non-deterministic finite automatas (NFAs) which are implemented on the FPGA.

PROFESSIONAL EXPERIENCE

Microsoft Research June 2018 - September 2018
Research Intern *Cambridge, UK*

· Design and implementation of a hardware prototype of a graph database for an FPGA-based distributed system.

Microsoft Research June 2015 - August 2015
Research Intern *Redmond, WA*

· Development of a debugging framework for FPGA-based soft processors in the context of Cipherbase.

Xilinx Research Lab May 2013 - February 2014
Research Intern *Dublin, Ireland*

· Development and implementation of a scalable 10 Gbps TCP/IP stack for FPGAs using high-level synthesis.

SixTelekurs (SixGroup) September 2010 - February 2011
Intern *Zürich, Switzerland*

· Evaluation of multiple in-memory data structures for a specific workload.

PEER-REVIEWED PUBLICATIONS

Z. He, D. Sidler, Z. Istvan, G. Alonso
A Flexible K-Means Operator for Hybrid Databases
FPL'18, Dublin, Ireland, 2018

Z. Istvan, D. Sidler, G. Alonso
Active Pages 20 Years Later: Active Storage for the Cloud
IEEE Internet Computing July/Aug 2018

Z. Istvan, D. Sidler, G. Alonso
Caribou: Intelligent Distributed Storage
VLDB'17, Munich, Germany, 2017

D. Sidler, Z. Istvan, M. Owaida, G. Alonso
Accelerating Pattern Matching Queries in Hybrid CPU-FPGA Architectures
SIGMOD'17, Chicago, IL, 2017

M. Owaida, D. Sidler, K. Kara, G. Alonso
Centaur: A Framework for Hybrid CPU-FPGA Databases
FCCM'17, Napa, CA, 2017

D. Sidler, K. Eguro
Debugging Framework for FPGA-based Soft Processors
FPT'16, Xi'an, China, 2016

D. Sidler, Z. Istvan, G. Alonso
Low-Latency TCP/IP Stack for Data Center Applications
FPL'16, Lausanne, Switzerland, 2016

Z. Istvan, D. Sidler, G. Alonso
Runtime Parameterizable Regular Expression Operators for Databases
FCCM'16, Washington DC, 2016

Z. Istvan, D. Sidler, G. Alonso, M. Vukolic
Consensus in a Box: Inexpensive Coordination in Hardware
NSDI'16, Santa Clara, CA, 2016

D. Sidler, M. Blott, K. Karras, R. Carley, G. Alonso, K. Vissers
Scalable 10 Gbps TCP/IP Stack Architecture for Reconfigurable Hardware
FCCM'15, Vancouver, Canada, 2015

DEMOS

D. Sidler, M. Owaida, Z. Istvan, K. Kara, G. Alonso
doppioDB: A Hardware Accelerated Database
SIGMOD'17 and FPL'17

Z. Istvan, D. Sidler, G. Alonso
Building a Distributed Key-value Store with FPGA-based Micro-servers
FPL'15

INVITED TALKS

Hardware Acceleration at all levels
VMware, Palo Alto, CA, February 2017

Accelerating Pattern Matching Queries in Hybrid CPU-FPGA Architectures
University of Stanford, Stanford, CA, February 2017

Accelerating String Matching Queries with Hybrid CPU-FPGA Multicores
Oracle Labs, Redwood, CA, March 2016

Accelerating String Matching Queries with Hybrid CPU-FPGA Multicores
Intel Labs, Santa Clara, CA, March 2016

TEACHING EXPERIENCE

Teaching Assistant:

Advanced Systems Lab	Fall 2018, Fall 2017, Fall 2016
Data Modeling and Databases	Spring 2018, Spring 2014
Informatik II	Spring 2017, Spring 2016
Informationssysteme für Ingenieure	Fall 2016
Grundlagen der Informatik	Fall 2015
Programmieren und Problemlösen	Spring 2015

STUDENT MENTORING

Semester Project: Zhenhao He (co-supervised with Zsolt Istvan) *September 2017 - March 2018*
Title: A Flexible K-Means Operator for Hybrid Databases
The semester project contributed to a short paper at FPL'18

Bachelor Thesis: Patrizio Bonzani *September 2017 - January 2018*
Title: Fuzzy string matching on FPGAs

COMMUNITY SERVICE

Shadow PC Eurosys 2018

RESEARCH IMPACT

The TCP/IP stack I developed in collaboration with *Xilinx* was open sourced by *Xilinx* in September 2016 and continuously developed by me. A number of companies use the TCP/IP stack in their commercial products. For instance, *Arches Computing Systems* deployed it in a high-frequency application and *LegUp Computing* deployed in on Amazon's F1 instances in combination with a key-value store. Additionally, the open source stack is used in research projects such as IBM's *cloudFPGA* or the *Caribou* and *Enzian* project at ETH Zürich.

LANGUAGES

- German: Native
- English: Proficient
- French: Basic

REFERENCES

Available on request.